ABSTRACT

Logic apparatus filters noise signals on a signal line to a digital circuit. An edge detector determines one or more edges of the noise signals relative to a fast clock. Signals indicative of the edges asynchronously reset a timer; the timer clocks the latch of the signal line when the signal line is stable, and without noise signals detected by the edge detector, for a period defined by a slow clock. The slow clock is slower than the fast clock by several orders of magnitude. The edge detector may be constructed by one flip-flop and an XOR gate. A second flip flop couples to the signal line and the output of the timer to pass through the latched value of the signal line to the digital circuit when clocked by the timer.